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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,444	03/25/2004	Hiroki Hiyama	03500.017982.	4861

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FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
WANG, KENT F	

ART UNIT	PAPER NUMBER
2609	

MAIL DATE	DELIVERY MODE
05/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/808,444	HIYAMA ET AL.	
	Examiner	Art Unit	
	Kent Wang	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/27/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The reference listed on the disclosure statement (IDS) submitted on 05/27/2004 has being considered by the examiner (see attached PTO 1449).

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. The abstract of the disclosure is objected to because abstract should be mentioned correction data to correct the noise components which are generated by the clamping circuits because that is what the improvement the invention is disclosed. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-9 are rejected under 35 U.S.C. § 102(b) as being anticipated by Tashiro, US 2002/0190215.

Regarding claim 1, Tashiro discloses an image pickup apparatus comprising:

- a plurality of pixels (i.e. image pickup elements 100, figure 10 is a circuit diagram of one pixel) each including a photoelectric converting element (i.e. photodiode PD for performing photoelectric conversion) (see [0049] and [0074]);
- a plurality of capacitor (i.e. capacitor C_{PD} and capacitor C_{FD}) which receive signals from said plurality of pixels at first terminals (i.e. ϕRES and ϕSEL from vertical scanning circuit) (see [0074] and figure 10);
- a plurality of clamping switches (i.e. a transfer switch M1, a reset switch M2, and a selection switch M3) for setting a second terminal of each of said plurality of capacitor (i.e. C_{PD} and C_{FD}) into a predetermined electric potential ([0074]);
- a plurality of first storing units (i.e. switch M8 plus holding capacitor CH1) for storing signals from said second terminals of said plurality of capacitor ([0075] and figure 10);
- a plurality of second storing units (i.e. switch M11 plus holding capacitor CH2) for storing the signals from said second terminals of said plurality of capacitor ([0075] and figure 10);

- a first common output line to which the signals from said plurality of first storing units are sequentially output (e.g. output it to a signal line; [0075] line 11 and figure 10);
- a second common output line to which the signals from said plurality of second storing units are sequentially output (e.g. output it to a signal line; [0075] line 39 et seq and figure 10); and
- a difference circuit (i.e. differential amplifier A1) for operating a difference between the signal from said first common output line and the signal from said second common output line (e.g. an optical signal and a noise signal from each pixel are outputted to the differential amplifier A1; [0087] lines 10-13).

Regarding claim 2, Tashiro discloses each of plurality of pixels includes a first amplifying element (i.e. an amplification MOS transistor M4) for amplifying and outputting a signal from said photoelectric converting element (PD) and a reset switch (M2) for resetting an input portion of said first amplifying element ([0074]).

Regarding claim 3, Tashiro discloses a second amplifying element (i.e. pixel amplifiers 2 and 3) for amplifying and outputting the signal from the second terminal of capacitor, and wherein the signal from the second amplifying element is transferred to first storing unit and second storing unit (e.g. M9 and M12 are MOS transistors as selection switches of the pixel amplifiers 2 and 3) ([0075]).

Regarding claim 4, Tashiro discloses first storing unit includes a first transfer gate (M1) and a first holding capacitor (CH1) for holding the transferred signal, and said

second storing unit includes a second transfer gate (M11) and a second holding capacitor (CH2) for holding the transferred signal, and

- wherein said image pickup apparatus further comprises a driving circuit (i.e. figure 12) arranged so that after said clamping switch (M1) is turned off at a first timing, said clamping switch is continuously held in an OFF state (e.g. M1 is in an OFF state during an accumulation period) and said first transfer gate is closed at a second timing (e.g. photocharges are not transferred; [0088] lines 9-12), thereby holding a first signal which is obtained from said second terminal of said capacitor into said first holding capacitor, and after said clamping switch is turned off at the first timing, said clamping switch is continuously held in the OFF state and said second transfer gate is closed at a third timing (e.g. photocharges are not transferred), thereby holding a second signal which is obtained from said second terminal of said capacitor into said second holding capacitor (e.g. M1 is turned on to completely transfer the electric charges accumulated in the photodiode; [0089]).

Regarding claim 5, Tashiro discloses a driving circuit effects driving so that the second terminal of said capacitor (C_{FD}) is set into said predetermined electric potential (ϕRES) by turning on said clamping switch (M1), the signal which is obtained from said first amplifying element (M4) by resetting the input portion of said first amplifying element (M4) is transferred to the first terminal of said capacitor (C_{PD}), said clamping switch (M1) is turned off and thereafter said first signal which is obtained from the

second terminal of said capacitor (C_{FD}) is held in said first storing unit, after that, a signal, which is output from said first amplifying element (M4), including the photoelectric conversion signal (ϕTX) from said photoelectric converting element (PD) is transferred to the first terminal of said capacitor (C_{PD}), and said second signal which is obtained from the second terminal of said capacitor (C_{FD}) is held in said second storing unit (M11 + CH2) ([0074] and [0075]).

Regarding claim 6, Tashiro discloses a driving circuit effects driving so that the second terminal of said capacitor (C_{FD}) is set into said predetermined electric potential (ϕRES) by turning on said clamping switch (M1), then a signal, which is output from said second amplifying element (i.e. pixel amplifiers 2 and 3), including the photoelectric conversion signal (ϕTX) from said photoelectric converting element (PD) is transferred to the second terminal of said capacitor (C_{FD}), said clamping switch (M1) is turned off and thereafter said first signal which is obtained from the second terminal of said capacitor (C_{FD}) is held in said first storing unit (M8 + CH1), the signal which is obtained from said second amplifying element (pixel amplifiers 2 and 3) by resetting the input portion of said second amplifying element (pixel amplifiers 2 and 3) is transferred to the first terminal of said capacitor (C_{PD}), and said second signal which is obtained from the second terminal of said capacitor (C_{FD}) is held in said second storing unit (M11 + CH2) ([0074] and [0075]).

Regarding claim 7, Tashiro discloses a plurality of pixels (100) are two-dimensionally arranged in a horizontal direction and a vertical direction (e.g. arranged in a two-dimensional state; [0049]),

- wherein said image pickup apparatus (i.e. image pickup element unit 112) further comprises an analog/digital converting circuit (i.e. A/D converter 113) for converting a signal output from said difference circuit into a digital signal and a correcting circuit (i.e. image processing circuit 116) for correcting the signal from said analog/digital converting circuit, and
- wherein said correcting circuit (116) has one-dimensional correction data (i.e. a signal ϕSEL1) and corrects the signals from said plurality of pixels arranged two-dimensionally (100) on the basis of said one-dimensional correction data (see [0153] and figure 23).

Regarding claim 8, Tashiro discloses a correction data includes noise components, which are generated in the case of turning off said clamping switch (e.g. transfer switch M1 is turned off to change a signal ϕSEL1 from the vertical shift register VSR to high level collectively for all the pixels as indicated in figure 12; see [0089]).

Regarding claim 9, Tashiro discloses a correction data includes noise components which are generated in the case of turning off said second amplifying element (e.g. a signal ϕSEL2 is changed to high level for each column by a signal inputted in the vertical shift register VSR, then the second amplifying element, M9 and M12, are turned on to bring the source follower circuit constituted of the load current source and the pixel amplifiers 2 and 3; see [0092] lines 1-7).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

   - Miyamoto (US 6,975,356) disclose a solid-state imaging device reduces fixed pattern noise (FPN) and thermal noise.
   - Funakoshi (US 6,498,332) disclose a solid-state image sensing device, which can perform a high-speed read while ensuring low power consumption and wide dynamic range can be implemented.
   - Watanabe (US 6,734,908) discloses an invention provides a correlated double sampling circuit that can provide an amplification type solid state imaging device capable of remarkably reducing FPN.
   - Inui (US 6,801,255) disclose a solid-state imaging device obtains a high-quality image by accurately removing an offset generated between a plurality of channels.

Inquiries

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kent Wang whose telephone number is 571-270-1703. The examiner can normally be reached on 8:00 A.M. - 5:30 PM (every other Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on 571-272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-270-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kent Wang

9 May 2007

CHANH D. NGUYEN
SUPERVISORY PATENT EXAMINER